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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :
ERIC J STRANG : EXAMINER: SIEK, VUTHE
SERIAL NO: 10/673,506 :
FILED: SEPTEMBER 30, 2003 : GROUP ART UNIT: 2825
FOR: SYSTEM AND METHOD FOR :
USING FIRST-PRINCIPLES SIMULATION
TO ANALYZE A PROCESS PERFORMED
BY A SEMICONDUCTOR PROCESSING
TOOL

REPLY BRIEF UNDER 37 CFR 41.41

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is a Reply Brief to the Examiner's Answer dated October 31, 2008.

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I. Status of Claims

Claims 1-62 and 66-68 are pending and appealed. Claims 63-65 and 69 have been canceled.

Claim 66 stands rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Claims 1-25, 32-56 and 63-69 stand rejected under 35 U.S.C. § 103(a) as being obvious over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Kee et al (U.S. Pat. No. 5,583,780). Claims 26-31 and 57-62 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al and Kee et al in view of Fatke et al (U.S. Pat. Appl. No. 2005/0016947).

II. Grounds of Rejection for Review

Whether the rejection of Claim 66 under 35 U.S.C. § 101 should be reversed.

Whether the rejection of Claims 1-25, 32-56 and 63-69 under 35 U.S.C. § 103(a) as being obvious over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Kee et al (U.S. Pat. No. 5,583,780) should be reversed. Whether the rejection of Claims 26-31 and 57-62 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al and Kee et al in view of Fatke et al (U.S. Pat. Appl. No. 200510016947) should be reversed.

III. Arguments

A. Regarding the 35 USC 103 Rejection of Claim 1-25, 32-56 and 63-69 over Sonderman et al and Kee et al

Claim 1 defines:

1. A method for analyzing a process performed by a semiconductor processing tool, comprising:
inputting process data relating to an actual process being performed by the semiconductor processing tool;
inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;
performing a first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, *said first principles simulation result being produced in a time frame shorter in time than the actual process being performed;* and
using the first principles simulation result *obtained during the performance of the actual process* to determine a fault in the actual process being performed by the semiconductor processing tool. [Emphasis added.]

The Examiner and the Appellant continue to disagree as to whether Sonderman et al teach performing a first principles simulation for an actual process being performed to provide a first principles simulation result in order to simulate the actual process being performed.

In particular, the Examiner appears to be now relying heavily on Figure 1 of Sonderman et al. The Examiner characterized Sonderman et al by stating on page 13 of the Examiner's Answer that "the simulation environment 210 (simulation environment 210 shown in Fig. 1) can emulate the operation of an actual process control environment 180." The Examiner also characterized Sonderman et al's Figure 1 by stating on page 14 of the Examiner's Answer that "Fig. 1 explicitly shown the actual process is performed (actual

process performed by manufacturing processes using processing tools A and B); then the process data is forwarded to the simulation environment 210 shown [arrow from processing tools to simulation environment] in Fig. 1.” Thereafter, the Examiner stated that “it is clearly that the principled simulation is performed for the actual process being performed during performance of the actual process because it is the integrated system that provides interactions between the components shown in Fig. 1, 2, and 3.”

Figure 1 of Sonderman et al is reproduced below.

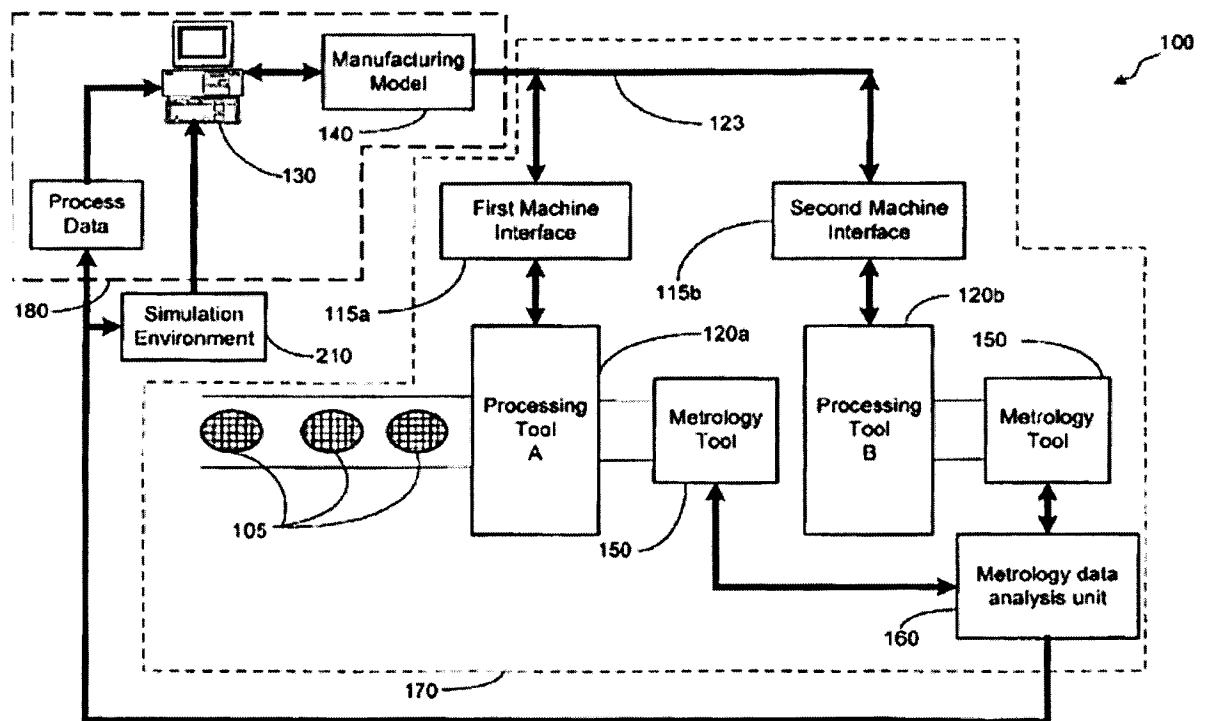


FIGURE 1

Appellant respectfully points out that, at col. 4, line 48, to col. 5, line 10, Sonderman et al specifically states:

Referring now to FIGS. 1 and 2 simultaneously, one embodiment of an interaction between a process control environment 180, a manufacturing/processing environment 170, and a simulation environment 210

is illustrated. In one embodiment the process control environment 180 receives input data from the simulation environment 210, which is then used to control the operation of the manufacturing environment 170. The integration of the simulation environment 210 and the process control environment 180 into the manufacturing environment 170 facilitates more accurate control of the processing of semiconductor wafers. The simulation environment 210 allows for testing various manufacturing factors in order to study and evaluate the interaction between the manufacturing factors. This evaluation can be used by the system 100 to prompt the process control environment 180 to invoke more accurate process control.

Furthermore, the simulation environment 210 can be used for feedback modification of control parameters invoked by the process control environment 180. For example, the manufacturing environment 170 can send metrology data results into the simulation environment 210. The simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180. A feedback loop is then completed when the process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers.

Appellants point out that there is no disclosure here of the claimed performing a first principles simulation for *the actual process being performed* to provide a first principles simulation result in order to simulate the actual process being performed.

Reiterating in part, Claim 1 defines:

inputting process data relating to an actual process being performed by the semiconductor processing tool;

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performing a first principles simulation for the actual process being performed to provide a first principles simulation result in order to simulate the actual process being performed.

Thus, for Sonderman et al to meet these claim elements, Sonderman et al would have to show input data from the process being directly used by the computer system 130 to compute a simulation result. Yet, Figure 1 of Sonderman et al shows the only input to the computer system 130 is by way of metrology data.

Metrology data is data taken on samples after a process has been performed. See Appellant's specification numbered paragraph [0106] for a listing of metrology data taken on a sample from "a process performed by semiconducting processing tool 102." Indeed, the second part of the noted above quote from Sonderman et al, states with regard to metrology data and feedback control that:

The simulation environment 210 can then use *the metrology data results* and perform various tests and calculations to provide more accurate, *modified control parameters* to the process control environment 180. A *feedback loop* is then completed when the process control environment 180 sends the *modified or adjusted process control parameters* to the manufacturing environment 170 *for further processing* of semiconductor wafers.

If Sondermann et al were able to obtain metrology data on the actual process being performed, Sondermann et al would not have to restrict the use of metrology data to feedback control, but rather could use the metrology data for feedforward control.

More significantly, Appellant's position on this matter is corroborated by col. 4, lines 31-47, of Sonderman et al which specifically states:

One or more of the semiconductor wafers 105 *that are processed* by the processing tools 120a, 120b can also be sent to a metrology tool 150 for acquisition of metrology data. The metrology tool 150 can be a scatterometry data acquisition tool, an overlay-error measurement tool, a critical dimension measurement tool, and the like. In one embodiment, *one or more processed semiconductor wafers are examined* by the metrology tool 150. Data from the metrology tool 150 is collected by a metrology data analyzer unit 160. The metrology data analyzer unit 160 organizes, analyses, and correlates scatterometry metrology data acquired by the metrology tool 150, to particular semiconductor wafers 105 that were examined. The metrology data analyzer unit 160 can be a software unit, a hardware unit, or a firmware unit. In one embodiment, the metrology data analyzer unit 160 is integrated into the computer system 130.

Appellant's position on this matter is also corroborated by col. 9, lines 46-51, of Sonderman et al which specifically states:

The system 100 **then** optimizes the simulation (described above) to find more optimal process target (T_i) for each silicon wafer, ***S_i to be processed***. These target values are then used to generate ***new control inputs, X_{Ti}*** , on the line 805 to control ***a subsequent process of a silicon wafer S_i*** . [Emphasis added]

The plain reading of this section of Sonderman et al is that the system 100 **then** (e.g., at time T1) optimizes the simulation for each silicon wafer, ***S_i to be processed*** (e.g., later at time T2). In other words, the simulation results of Sonderman et al produce a new control input for each silicon wafer ***to be processed***.

Thus, Appellant respectfully submits that Sonderman et al teach performing a simulation result for a process to be performed ***before*** performance of the actual process, and do **not** teach the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process***.¹

Other sections of Sonderman et al support Appellant's position on this matter that the simulation results in Sonderman et al are made prior to controlling a subsequent process. For instance, Figure 4 of Sonderman et al (reproduced below) shows that the simulation results are produced ***ahead of performing a process*** and thus are based on historical data.

¹ Appellant also points out that Sonderman et al do not disclose or suggest a first principles simulation.

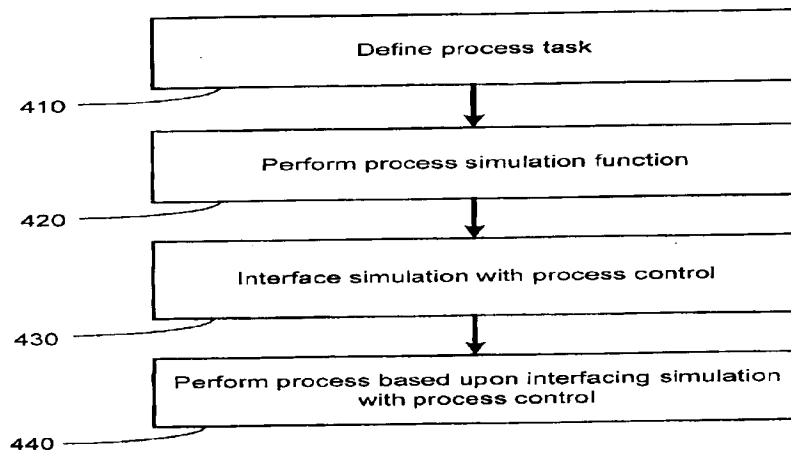


FIGURE 4

With reference to Figure 4, Sonderman et al disclose at col. 6, lines 24-47:

Turning now to FIG. 4, a flow chart representation of the methods in accordance with the present invention is illustrated. In one embodiment, *the system 100 defines a process task that is to be performed (block 410)*. The process task may be a photolithography process, an etching process, and the like. *The system 100 then performs a process simulation function (block 420)*. A more detailed description of the process simulation function described in block 420, is illustrated below. In one embodiment, a simulation data set results from the execution of the process simulation function.

Once the system 100 performs the process simulation function, the system 100 performs an interfacing function, which facilitates interfacing of the simulation data with the process control environment 180 (block 430). The process control environment 180 can utilize the simulation data in order to modify or define manufacturing control parameters that control the actual processing steps performed by the system 100. *Once the system 100 interfaces the simulation data with the process control environment 180, the system 100 then performs a manufacturing process* based upon the manufacturing parameters defined by the process control environment 180 (block 440). [Emphasis added]

Hence, the process flow in Sonderman et al is straightforward:

- 1) define a process to be modeled,
- 2) model the simulation result,
- 3) interface simulation result to processor, and then

4) run the process under control based on the pre-existing simulation result.

Accordingly, Appellant respectfully submits that Sonderman et al do not disclose and indeed *teach away* from the present invention where data input from an actual process being performed is used for producing a first principles simulation result, which is produced for the actual process being performed during performance of the actual process in a time frame shorter in time than the actual process being performed.

Additionally, the Examiner takes a position in the Examiner's Answer (see pages 7 and 8) that:

The new added limitation, first principles simulation result being produced in a time frame shorter in time than the actual process being performed is obvious to artisan skill in the technological art. It is well known to artisan in the art that speed of processor used to run simulation determines a time frame to produce a simulation result.

Yet, this position presumes that the artisan could in fact make such a calculation in a time frame shorter in time than the actual process being performed.

The Examiner has provided no factual basis to support this position. Indeed, the Examiner needs to rely on obviousness from this assertion, because there is no support on the record that, prior to the invention, the artisan could have made such a first principles calculation in this time frame. The fundamental question is whether there are technological difficulties which prohibit a person of ordinary skill in the art to obtain a simulation result in a time frame shorter in time than the actual process being performed. Appellants' specification states in numbered paragraph [0005] that:

Indeed, the failure of industry to implement on-tool simulation to facilitate tool processes is primarily due to the need for computational resources capable of performing the simulations in a reasonable time.

The Examiner in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Kee et al for their teaching of computer encoded differential equations.

However, as explained below, these teachings of Kee et al also corroborate Appellant's position on this matter.

Kee et al deal with the process control of a Rapid Thermal Processing (RTP) tool and do **not** use real time modeling. RTP tools are tools used in semiconductor manufacturing. Kee et al in detail disclose that:

The modeling apparatus 101 of the instant invention may also be used to perform an inverse analysis to establish the boundary conditions or parameter values required to achieve a certain function of the thermal system. This allows the apparatus to be used to establish the appropriate process parameters and boundary conditions for the thermal system modeled. In accordance with the instant invention, the inverse analysis can be directly carried out by the modeling apparatus *rather than using the conventional approach, which merely solves the direct problem repeatedly, in a lengthy and costly iterative process*, to determine appropriate input parameters to achieve a desired result. In other words, in accordance with the instant invention, *once a particular thermal process is modeled for a particular set of control parameters*, the device may then be used to automatically obtain the necessary control parameters to achieve a desired result by providing the modeling apparatus with parameters corresponding to the desired result.

To carry out the inverse analysis, the modeling apparatus 101 includes an inverse parameter input section 104 also connected to input device 103. A user inputs into the modeling apparatus 101 parameters corresponding to desired results, e.g., desired temperature characteristics of the system, which are stored in memory 108. The processing unit 110, under control of modeling program 111, *uses the previously generated model* of the thermal system and the parameters held in memory 108 and derives or predicts particular control parameters to meet the constraints entered through the inverse parameter input section 104. This process is more fully described below in connection with the examples provided.² [Emphasis added.]

Hence, Kee et al explicitly disclose that a *previously generated* model of the thermal system is used to design and control the thermal system. Kee et al exemplify the difficulties of a "conventional approach" which solves spectral radiation transport equations through "a lengthy and costly iterative process." These problems forced Kee et al to use *pre-generated model results* for control of a RTP process.

² Kee et al, col. 4, lines 21-50.

Hence, Kee et al. further Appellant's position on non-obviousness by illustrating the technological difficulty of producing a first principle simulation result in a time frame shorter in time than the actual process being performed.

For all these reasons, Appellant submits that Claims 1, 8, and 75 patentably define over Sonderman et al and Kee et al.

Hence, the 35 U.S.C. § 103(a) rejection of Claims 1-25, 32-56 and 63-69 as being unpatentable over Sonderman et al and Kee et al should be reversed.

B. Regarding the 35 U.S.C. § 103 Rejection of Claims 26-31 and 57-62 over Sonderman et al, Kee et al, and Fatke

The February 19, 2008 Office Action applied Fatke et al to overcome the deficiencies of Sonderman et al regarding the features of Claims 26-31 and 57-62. The Office Action stated at page 11:

Sonderman et al. do not explicitly teach the multivariate analysis comprising a partial least square analysis; defining a set of loading coefficients, computing at least one of mean and standard deviation values. Fatke et al. teach these limitations including defining a correlation matrix in order to improve detection of a feature etch completion process during semiconductor manufacturing to thereby providing accurate and precise completion of an etch process (see abstract, Fig. 4, summary, 0051). Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine these teachings in to the system as taught by Sonderman et al. in order to provide an accurate and precise completion of a process during semiconductor manufacturing.

Yet, the examiner's position as to why it would have been obvious to combine Fatke et al with Sonderman et al is merely a conclusory statement with no articulated statement as to what features of Fatke et al and Sonderman et al would have to be modified to accept the endpoint detection of Fatke et al. KSR requires an articulated rationale as to why the claimed features are obvious and indicates that conclusory statements are not sufficient.

For the facts of the asserted obviousness rejection here, the endpoint detection of

Fatke et al is a plasma etch endpoint detection process. There is no disclosure in Sonderman et al of a plasma etching process. Thus, one does not know how extensively the processing tools A and B in Sonderman et al would have to be modified under the asserted combination postulated by the examiner. For example, Sonderman et al describe at col. 4, lines 18-30:

In one embodiment, the manufacturing model 140 defines a process script and input control that implement a particular manufacturing process. The control input signals on the line 123 that are intended for the processing tool A 120 a are received and processed by the first machine interface 115 a . The control input signals on the line 123 that are intended for the processing tool B 120 b are received and processed by the second machine interface 115 b. Examples of the processing tools 120a , 120b used in semiconductor manufacturing processes are steppers, scanners, step-and-scan tools, etch process tools, and the like. In one embodiment, the processing tool A 120a and the processing tool B 120b are photolithography process tools, such as steppers.

Later, at col. 6, lines 1-13, Sonderman et al describe that temperature changes in the equipment model cause changes to the etching process.

These descriptions imply that the etch process tools of Sonderman et al are photolithography etch tools (i.e., wet chemistry etch tools used to remove the exposed photoresist lines). The application of plasma diagnostics to wet chemistry tools (where plasmas are not used) would **not** lead to end point detection, even if the correlation matrix in Fatke et al were used. Further, converting a wet chemistry etch tool into a plasma etch tool would require considerable rework and redesign of the wet chemistry etch tool and would change its basic principle of operation from wet chemistry dissolution to dry gas etching.

The Examiner has made no attempt to address these points raised in the Appeal Brief. Rather, in the Examiner's Answer, the Examiner responds on page 17 by merely stating motivations for the asserted combination. Yet, even in these motivations, the Examiner states without proof for example that the "combination of teachings would provide an accurate and precise completion of a process during semiconductor manufacturing process." This

conclusion apparently does not take into consideration the above noted points that:

The application of plasma diagnostics to wet chemistry tools (where plasmas are not used) would **not** lead to end point detection, even if the correlation matrix in Fatke et al were used. Further, converting a wet chemistry etch tool into a plasma etch tool would require considerable rework and redesign of the wet chemistry etch tool and would change its basic principle of operation from wet chemistry dissolution to dry gas etching

Accordingly, as noted in the Appeal Brief, these facts are similar to In re Ratti, 270 F.2d 810, 813, 123 USPQ 349, 352 which reversed an obviousness rejection where the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate.

Thus, given these considerations, the rejections of Claims 26-31 and 57-62 should be reversed.

C. Regarding the 35 U.S.C. § 101 Rejection of Claim 66

Claim 66 defines:

A computer readable medium containing program instructions for execution on a processor, which when executed by the computer system, cause the processor to perform the steps of:

inputting process data relating to an actual process being performed by the semiconductor processing tool;

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;

performing a first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, said first principles simulation result being produced in a time frame shorter in time than the actual process being performed; and

using the first principles simulation result obtained during the performance of the actual process to determine a fault in the actual process being performed by the semiconductor processing tool.

M.P.E.P. 2106.01 indicates that:

When a computer program is claimed in a process where the computer is executing the computer program's instructions, USPTO personnel should treat the claim as a process claim.

Here, for Claim 66, the claimed computer readable medium contains program instructions for execution on a processor, which when executed by the computer system, cause the processor to perform the recited steps. Thus, this claim should be treated as a process claim.

Furthermore, given the recent decision of In re Bilski and Warsaw, (Fed. Cir. 2008), method claims define statutory subject matter if the subject matter as claimed (i.e., a computer readable medium) is tied to another statutory class. In this case, the claimed computer readable medium is tied to another statutory class - a processor. Moreover, Claim 66 defines that the computer readable medium is executable on a computer system, i.e., another statutory class. Moreover, Claim 66 defines steps of inputting data from a semiconductor processing tool and using a first principles simulation result to determine a fault in the actual process being performed by the semiconductor processing tool.

In re Bilski and Warsaw stated that

The Supreme Court, however, has enunciated a definitive test to determine whether a process claim is tailored narrowly enough to encompass only a particular application of a fundamental principle rather than to pre-empt the principle itself. A claimed process is surely patent-eligible under § 101 if: (1) it is tied to a particular machine or apparatus.

Here, in the present case, the computer readable medium is tied both to a processor, a computer system, and a semiconductor processing tool (all statutory categories). Therefore, Claim 66 is patent-eligible under § 101.

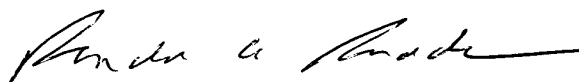
Hence, for these reasons, the 35 U.S.C. § 101 rejection of Claim 66 should be reversed.

VI. Conclusion

Appellant request on the basis of the arguments presented above that the outstanding grounds for the rejection be reversed. Appellant submits that the application is in condition for allowance.

Respectfully submitted,

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